Matt Keeter

matt.j.keeter@gmail.com Cambridge, MA
https://mattkeeter.com

EXPERIENCE

Sr. Software Engineer at Oxide Computer Co. 2021 - present
Developing low-level firmware and systems software for rack-scale servers and network switches, as part of a small, multi-disciplinary team. Working on a wide range of projects; on the low-level side, responsible for server thermal control and the bringup, control, and APIs for a custom 52-port, 80GiB network switch. Higher up the stack, optimized our backend storage system (improved architecture & data structures), yielding a 3-4× performance improvement. Writing primarily Rust, including reverse-engineering and porting C SDKs from vendors.

Sr. Electrical Engineer & Tech Lead at Formlabs, Cambridge MA 2013 - 2021
Held many roles as Formlabs grew from a 15-person 3D printing startup to a 600-person, $2B company. Developed desktop software (C++, Qt, OpenGL), PCBs (high-speed, mixed-signal), embedded software (Linux and bare-metal), across eight product lines with tens of thousands of units shipped to customers. Most recently, **tech lead** for two new product lines, leading 5-10 engineers (mechanical, electrical, software).

Independent Graphics Researcher, Cambridge MA 2013 - present
Playing with software and algorithms for designing with implicit surfaces. Developed `libfive`, an open-source library for solid modeling, which is now used in at least one commercial CAD package. Wrote a **single-author SIGGRAPH paper** on rendering complex implicit surfaces efficiently on modern GPUs.

Research Assistant, Cambridge MA Fall 2011 - Spring 2013
Worked at MIT's Center for Bits and Atoms on a wide variety of projects, including writing computation geometry engines and CAD software, designing and characterizing low-cost capacitive sensors, and testing propellor arrays in the wind tunnel.

Internship at MicroStrain, Burlington VT Summer 2011
Developed firmware for ultra low-power wireless sensor networks. Interfaced with 2.4 GHz IEEE 802.15.4 radio, low-power LCD display, and a variety of sensors.

Jackson Adders Research Project, Claremont CA Fall 2010 - Spring 2011
Led a team investigating Jackson's proposed adder optimization for high-speed computer arithmetic. Compared a variety of Jackson-style architectures against synthesized designs. First author on paper accepted to the Asilomar Conference on Signals, Systems, and Computers.

Project for National Optical Astronomy Observatory, Claremont CA Spring 2010
Designed a system for telescopes to improve image acquisition. Implemented firmware on an FPGA to sample, filter, and output pixels from a CCD.

RELEVANT SKILLS

C, C++, Python, Rust, shell scripting, Linux, CUDA, LaTeX
Prototyping & SMT soldering, PCB design, machining & fabrication

EDUCATION

Master of Science, Media Arts and Sciences (completed Spring 2013)
MIT, Cambridge MA GPA: 5.0/5

Bachelor of Science, Engineering (completed Spring 2011)
Harvey Mudd College, Claremont CA GPA: 3.93/4